ABSTRACT OF THE DISCLOSURE

The transposition circuit comprises N input terminals (where N is an integer of 2 or greater) and N output terminals. This transposition circuit is configured such that when N packets of data for each matrix row are inputted in parallel to the corresponding input terminals, N packets of data are outputted in parallel for each matrix column from the corresponding output terminals. This transposition circuit generates data packets arranged as a transposed matrix and obtained from data packets in the form of an N × N matrix by interchanging the rows and columns of the original matrix.